FIG. 1 (PRIOR ART)

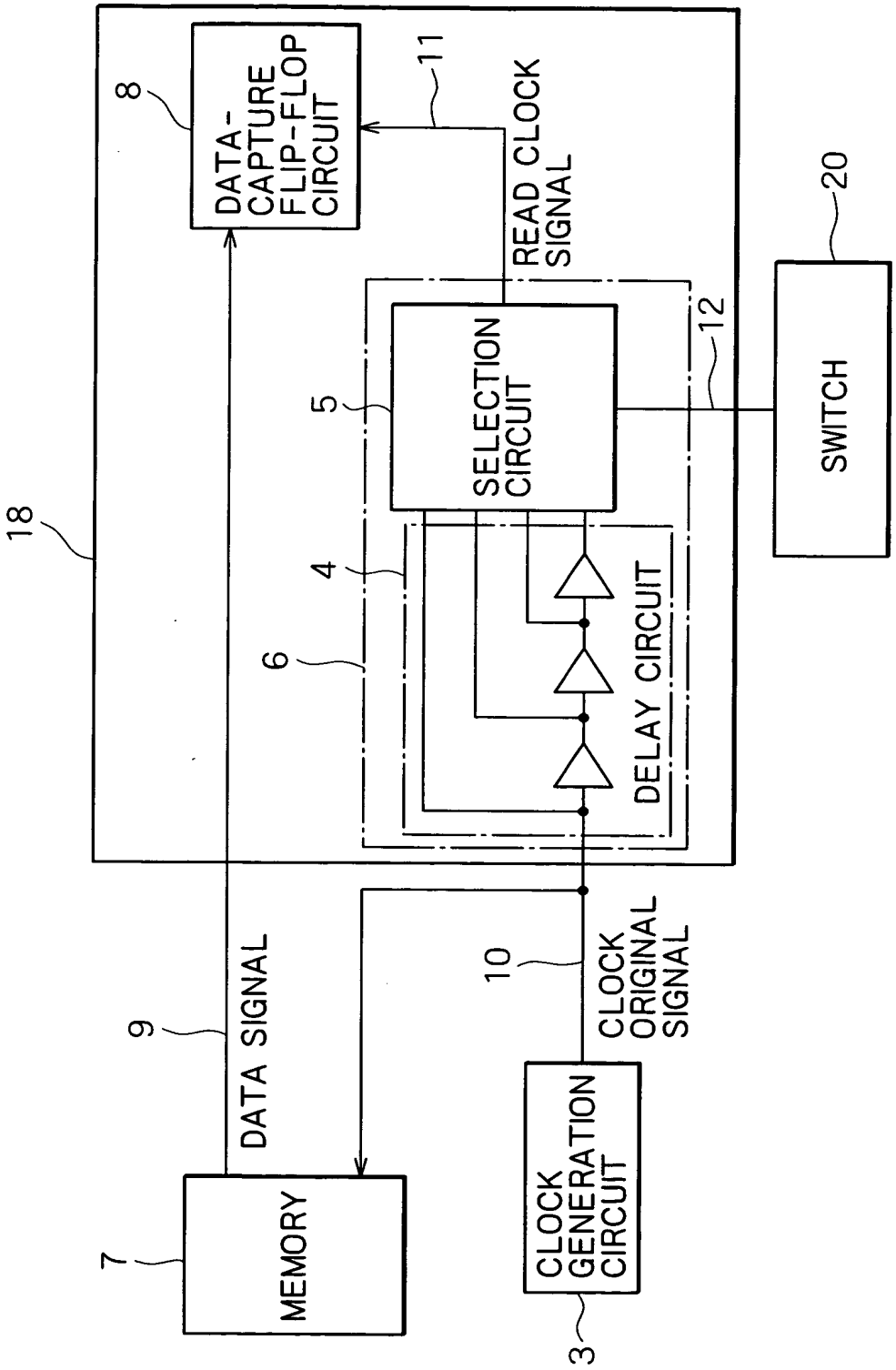


FIG. 2

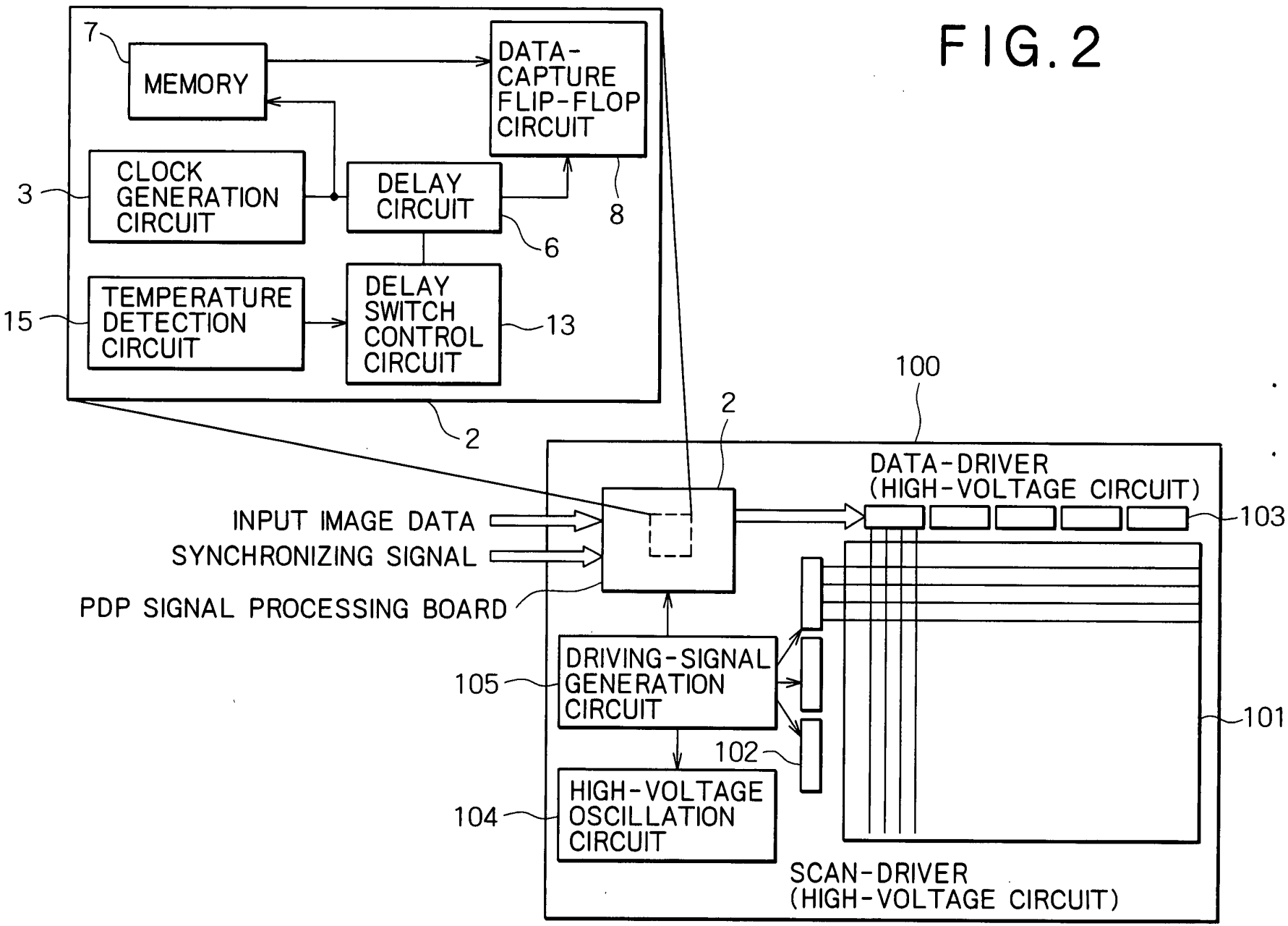

7
MEMORY
DATA-CAPTURE FLIP-FLOP CIRCUIT
8
3
CLOCK GENERATION CIRCUIT
DELAY CIRCUIT
6
15
TEMPERATURE DETECTION CIRCUIT
DELAY SWITCH CONTROL CIRCUIT
13
2
100
2
DATA-DRIVER (HIGH-VOLTAGE CIRCUIT)
103
INPUT IMAGE DATA
SYNCHRONIZING SIGNAL
PDP SIGNAL PROCESSING BOARD
105
DRIVING-SIGNAL GENERATION CIRCUIT
102
101
104
HIGH-VOLTAGE OSCILLATION CIRCUIT
SCAN-DRIVER (HIGH-VOLTAGE CIRCUIT)

FIG. 3

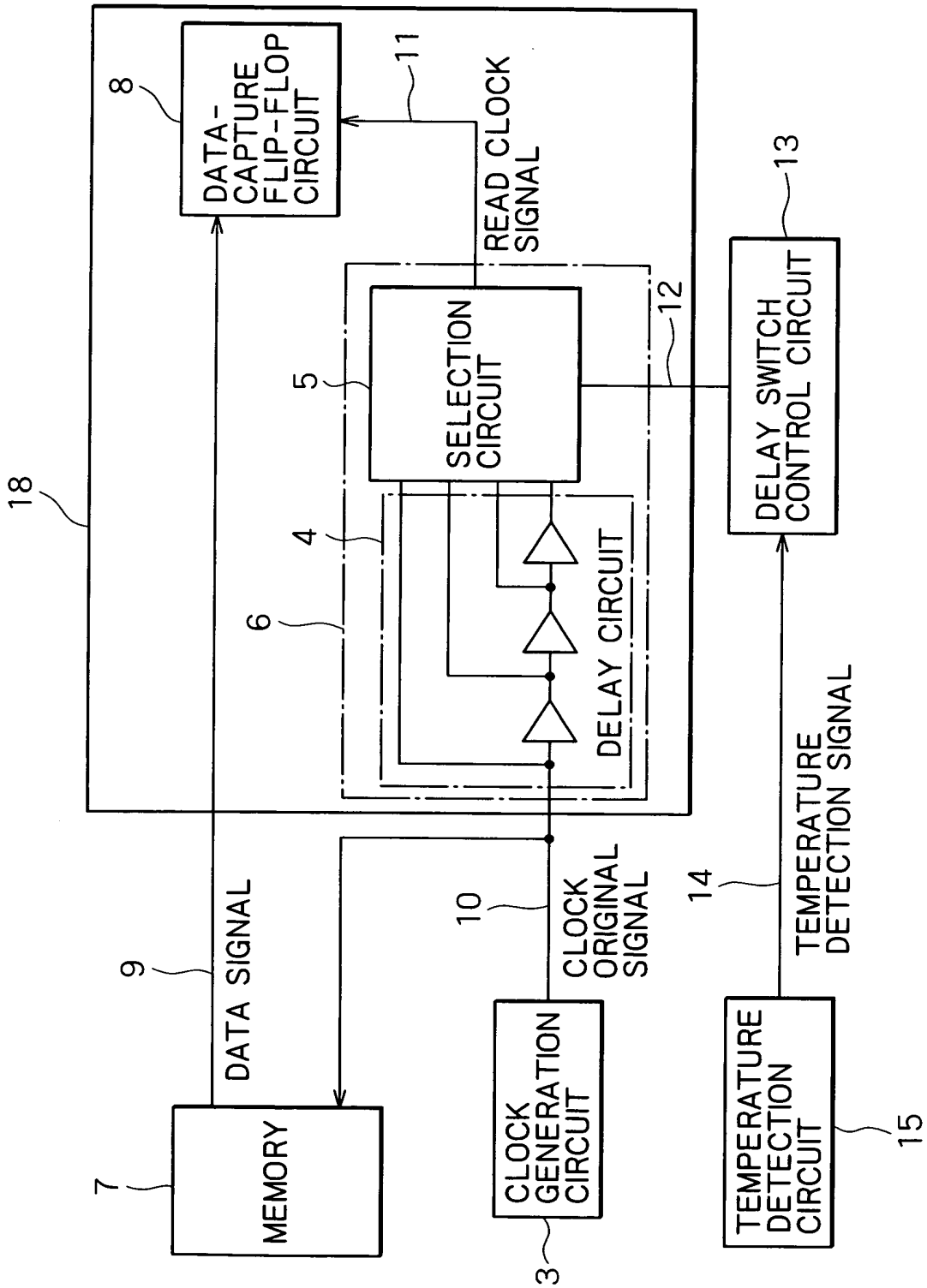

18
8
DATA-CAPTURE FLIP-FLOP CIRCUIT
11
READ CLOCK SIGNAL
13
DELAY SWITCH CONTROL CIRCUIT
5
SELECTION CIRCUIT
12
4
6
DELAY CIRCUIT
9
DATA SIGNAL
10
CLOCK ORIGINAL SIGNAL
14
TEMPERATURE DETECTION SIGNAL
7
MEMORY
CLOCK GENERATION CIRCUIT
3
TEMPERATURE DETECTION CIRCUIT
15

FIG. 4

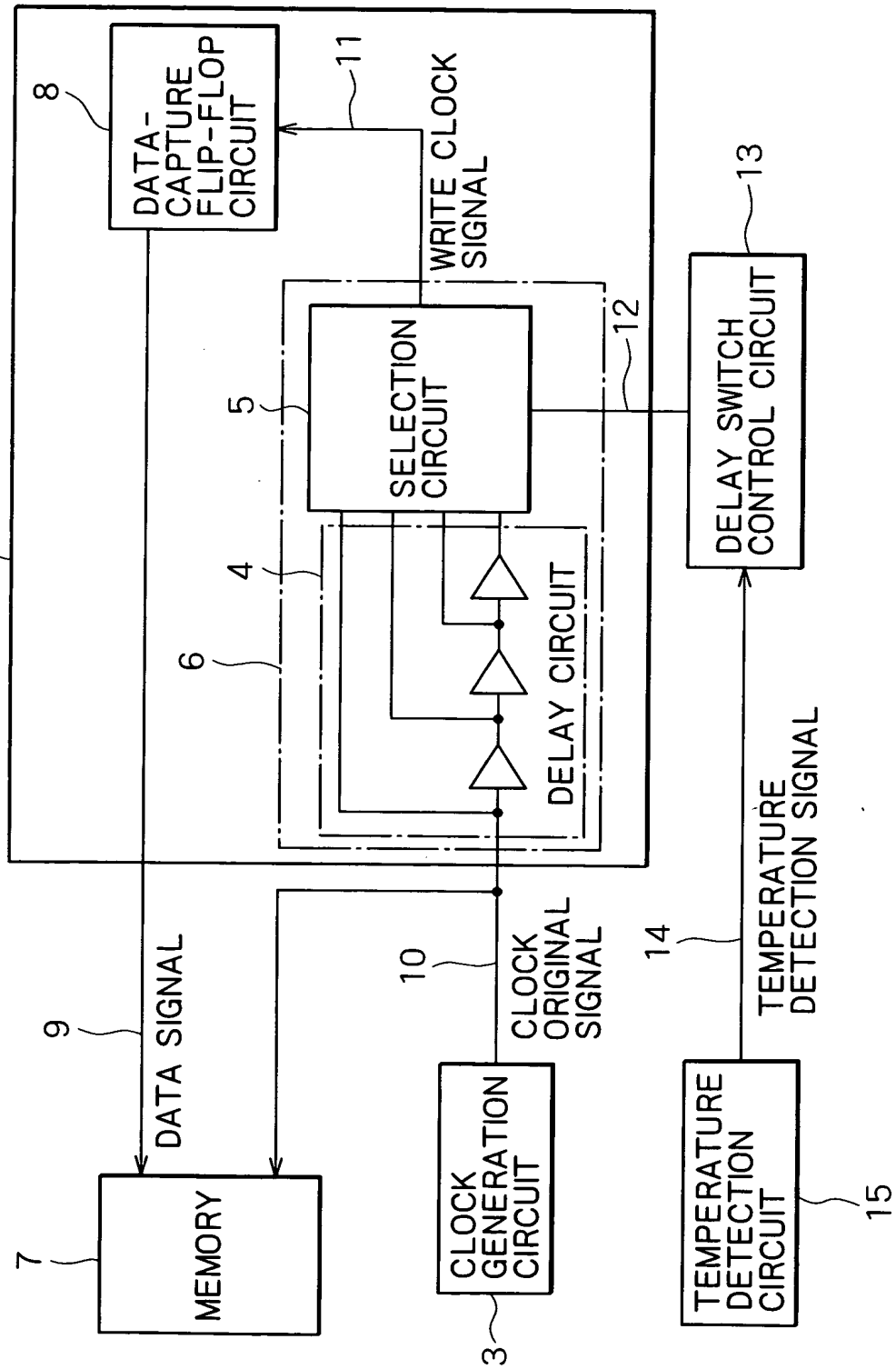

18
8
DATA-CAPTURE FLIP-FLOP CIRCUIT
11
WRITE CLOCK SIGNAL
5
SELECTION CIRCUIT
12
13
DELAY SWITCH CONTROL CIRCUIT
4
6
DELAY CIRCUIT
9
DATA SIGNAL
10
CLOCK ORIGINAL SIGNAL
14
TEMPERATURE DETECTION SIGNAL
7
MEMORY
CLOCK GENERATION CIRCUIT
3
TEMPERATURE DETECTION CIRCUIT
15

FIG. 5

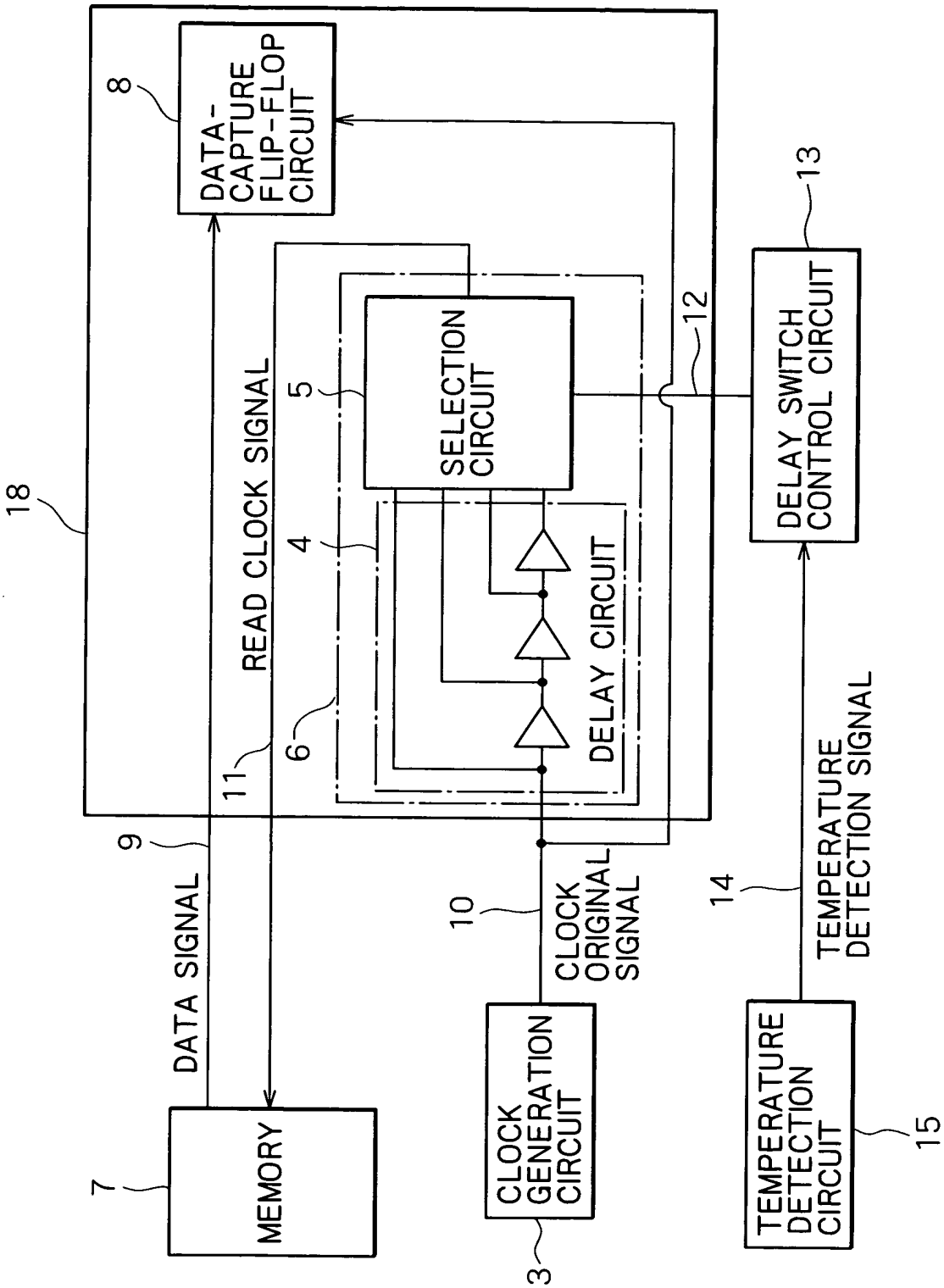

18
8
DATA-CAPTURE FLIP-FLOP CIRCUIT
READ CLOCK SIGNAL
5
SELECTION CIRCUIT
12
DELAY SWITCH CONTROL CIRCUIT
13
4
DELAY CIRCUIT
6
11
9
DATA SIGNAL
10
CLOCK ORIGINAL SIGNAL
14
TEMPERATURE DETECTION SIGNAL
7
MEMORY
CLOCK GENERATION CIRCUIT
3
TEMPERATURE DETECTION CIRCUIT
15

FIG. 6

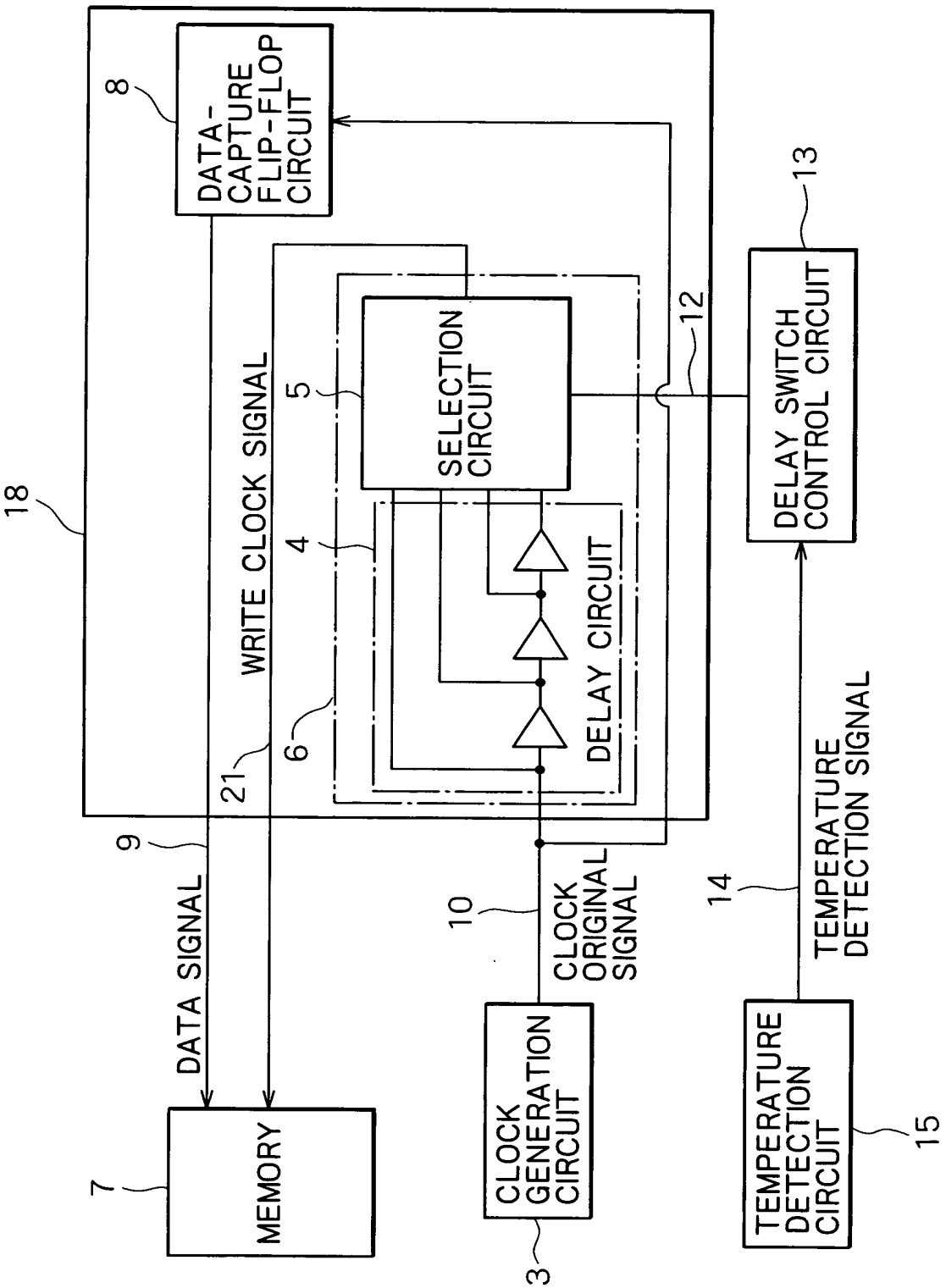

18
8
DATA-CAPTURE FLIP-FLOP CIRCUIT
WRITE CLOCK SIGNAL
21
5
SELECTION CIRCUIT
12
13
DELAY SWITCH CONTROL CIRCUIT
4
DELAY CIRCUIT
6
9
DATA SIGNAL
10
CLOCK ORIGINAL SIGNAL
14
TEMPERATURE DETECTION SIGNAL
7
MEMORY
CLOCK GENERATION CIRCUIT
3
TEMPERATURE DETECTION CIRCUIT
15

FIG. 7

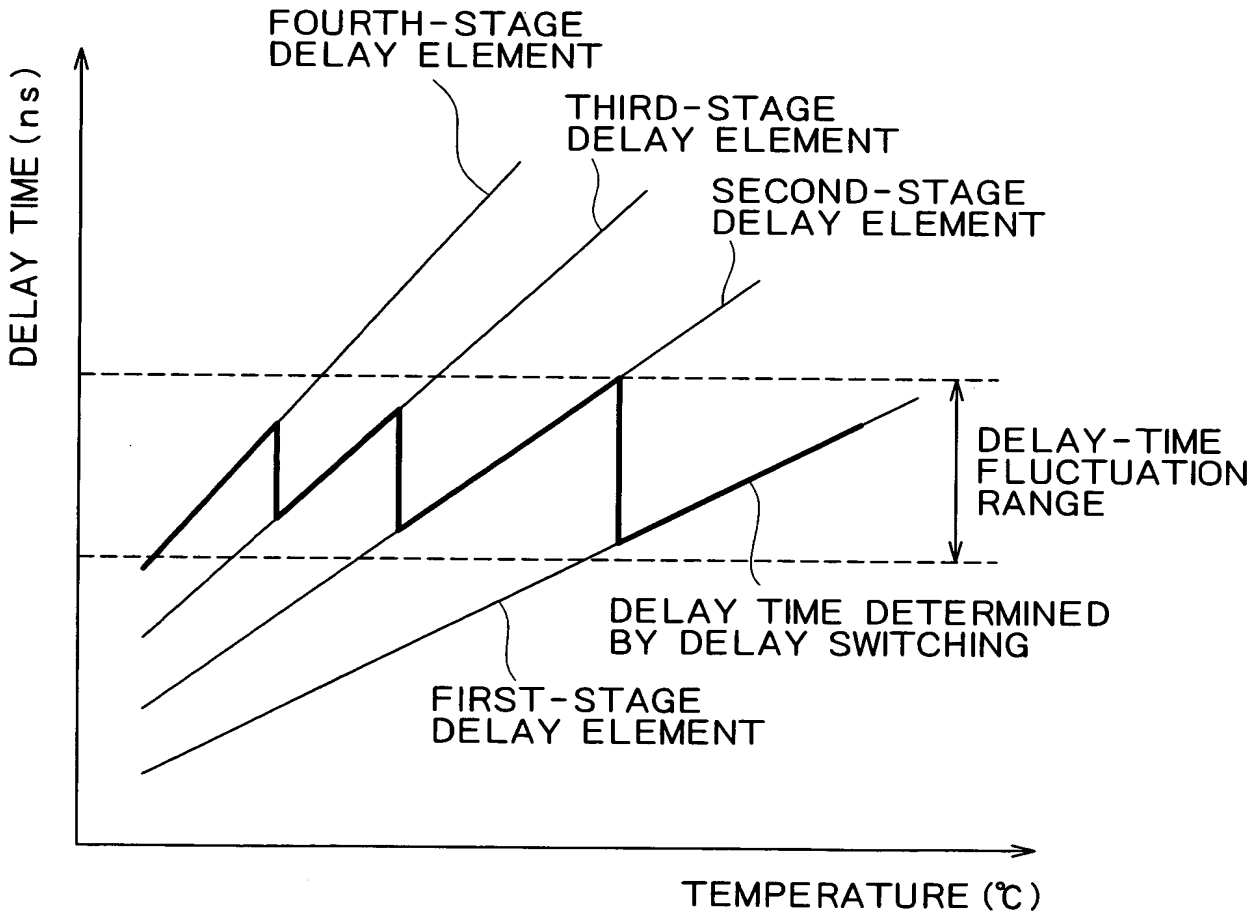

FOURTH-STAGE
DELAY ELEMENT
THIRD-STAGE
DELAY ELEMENT
SECOND-STAGE
DELAY ELEMENT
DELAY TIME (ns)
DELAY-TIME
FLUCTUATION
RANGE
DELAY TIME DETERMINED
BY DELAY SWITCHING
FIRST-STAGE
DELAY ELEMENT
TEMPERATURE (℃)

FIG. 8

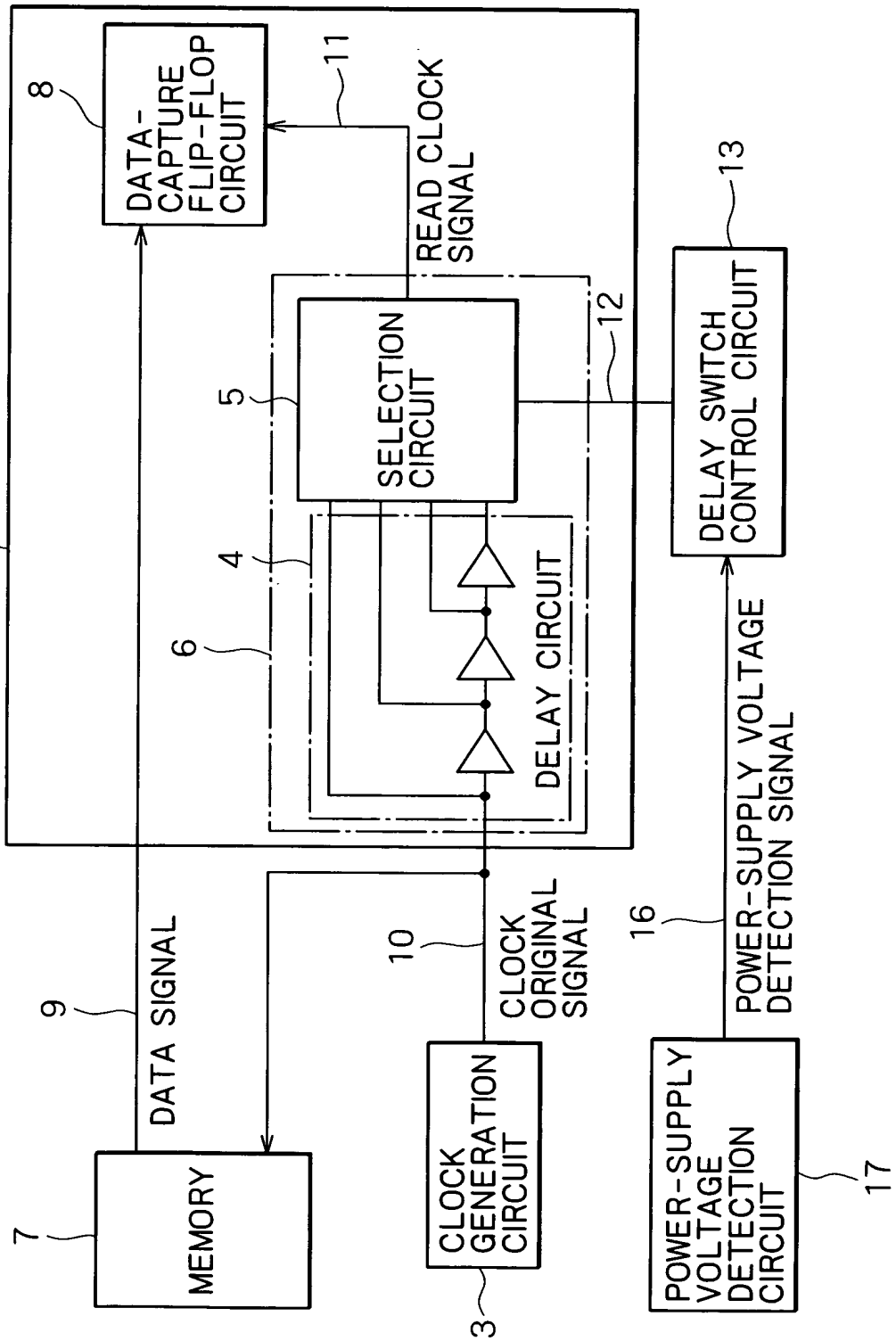

18
8
DATA-CAPTURE FLIP-FLOP CIRCUIT
11
READ CLOCK SIGNAL
5
SELECTION CIRCUIT
12
DELAY SWITCH CONTROL CIRCUIT
13
4
6
DELAY CIRCUIT
9
DATA SIGNAL
10
CLOCK ORIGINAL SIGNAL
16
POWER-SUPPLY VOLTAGE DETECTION SIGNAL
7
MEMORY
CLOCK GENERATION CIRCUIT
3
POWER-SUPPLY VOLTAGE DETECTION CIRCUIT
17

FIG. 9

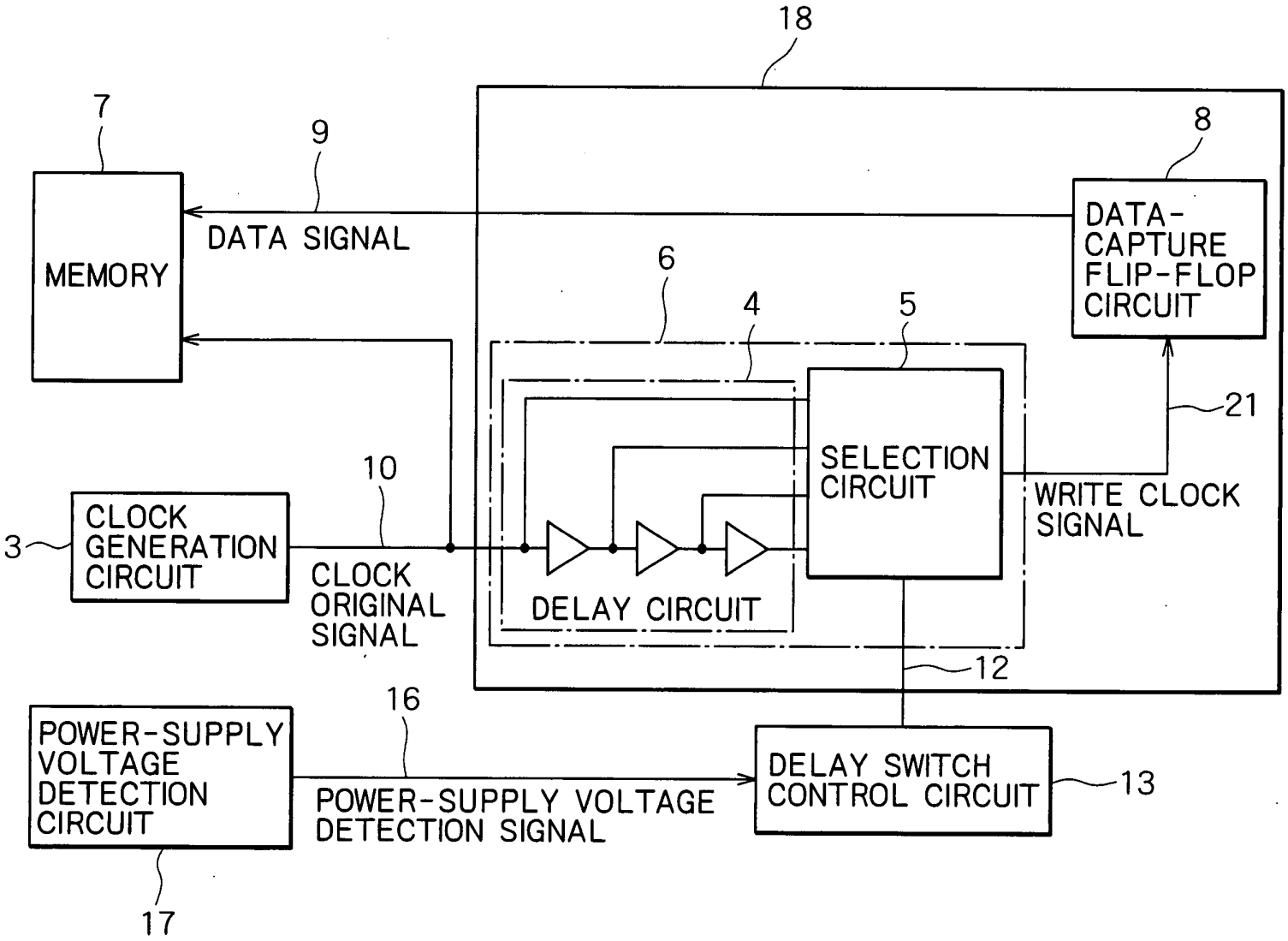

18
7
9
8
MEMORY
DATA SIGNAL
DATA-CAPTURE FLIP-FLOP CIRCUIT
6
4
5
21
SELECTION CIRCUIT
10
3
CLOCK GENERATION CIRCUIT
CLOCK ORIGINAL SIGNAL
WRITE CLOCK SIGNAL
DELAY CIRCUIT
12
16
POWER-SUPPLY VOLTAGE DETECTION CIRCUIT
DELAY SWITCH CONTROL CIRCUIT
13
POWER-SUPPLY VOLTAGE DETECTION SIGNAL
17

FIG. 10

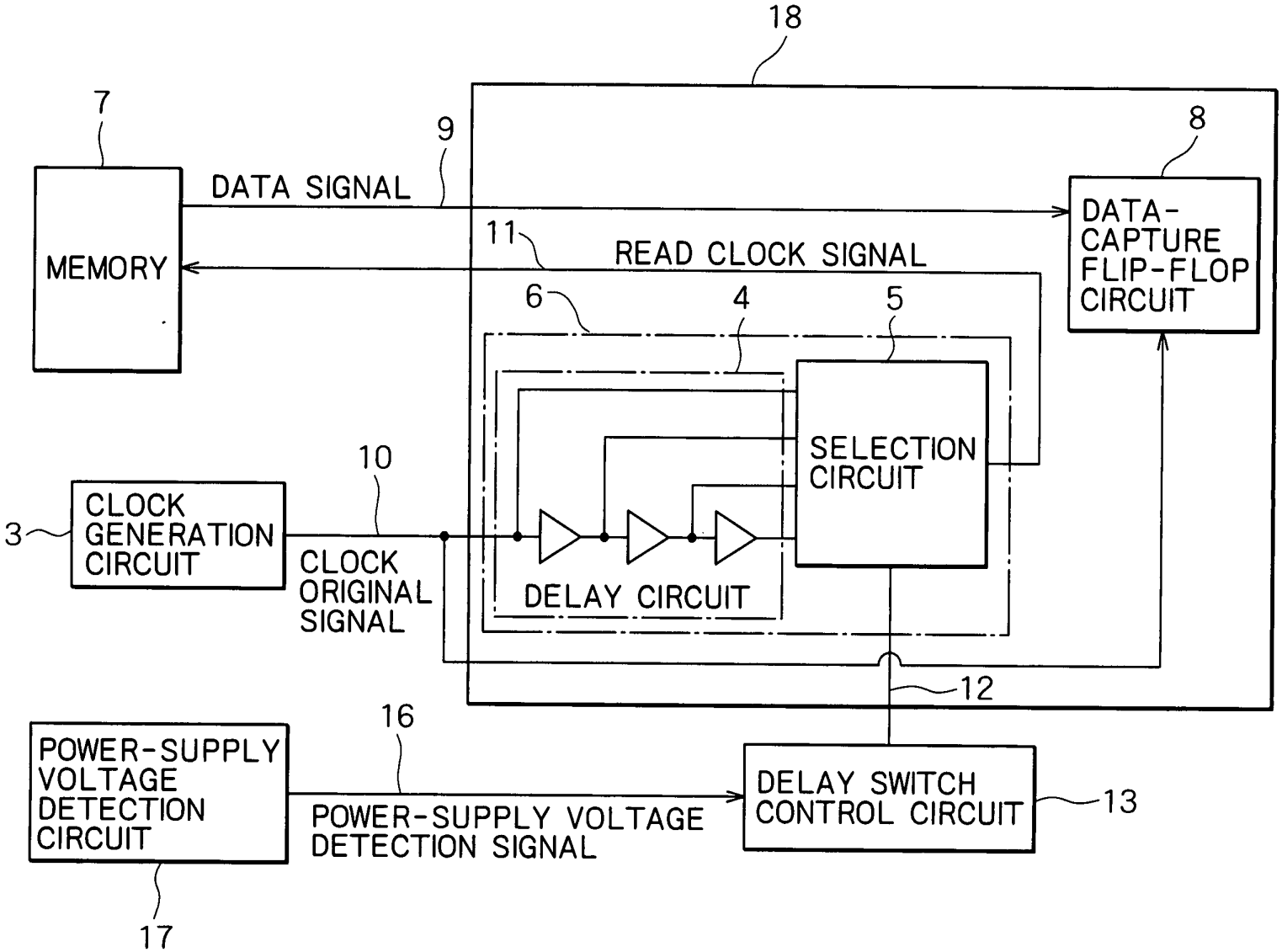

18
7
9
8
DATA SIGNAL
MEMORY
DATA-CAPTURE FLIP-FLOP CIRCUIT
11
READ CLOCK SIGNAL
6
4
5
SELECTION CIRCUIT
10
3
CLOCK GENERATION CIRCUIT
CLOCK ORIGINAL SIGNAL
DELAY CIRCUIT
12
16
POWER-SUPPLY VOLTAGE DETECTION CIRCUIT
POWER-SUPPLY VOLTAGE DETECTION SIGNAL
DELAY SWITCH CONTROL CIRCUIT
13
17

FIG. 11

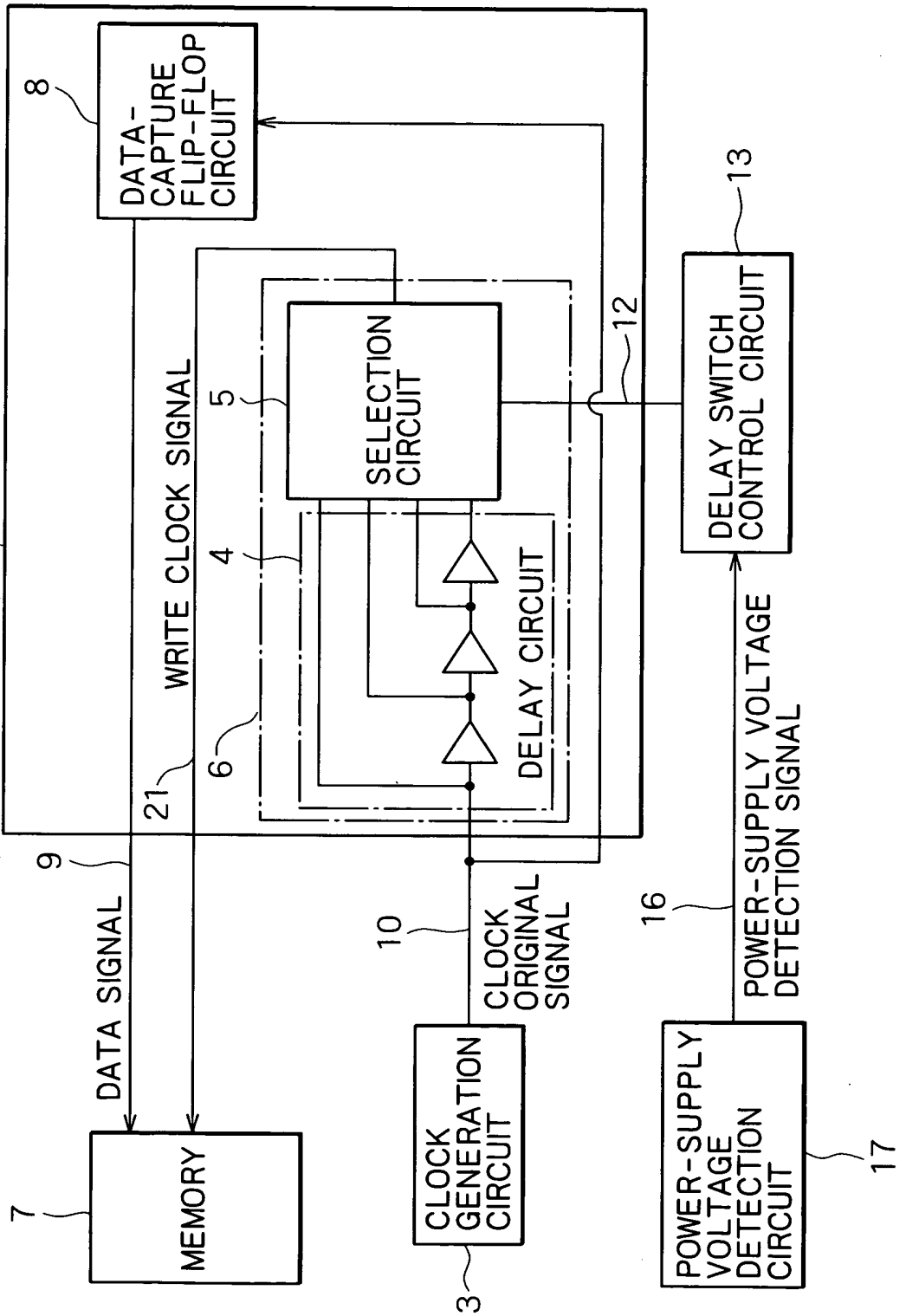

18
8
DATA-CAPTURE FLIP-FLOP CIRCUIT
WRITE CLOCK SIGNAL
21
5
SELECTION CIRCUIT
4
DELAY CIRCUIT
6
12
13
DELAY SWITCH CONTROL CIRCUIT
9
DATA SIGNAL
10
CLOCK ORIGINAL SIGNAL
16
POWER-SUPPLY VOLTAGE DETECTION SIGNAL
7
MEMORY
3
CLOCK GENERATION CIRCUIT
POWER-SUPPLY VOLTAGE DETECTION CIRCUIT
17

FIG. 12

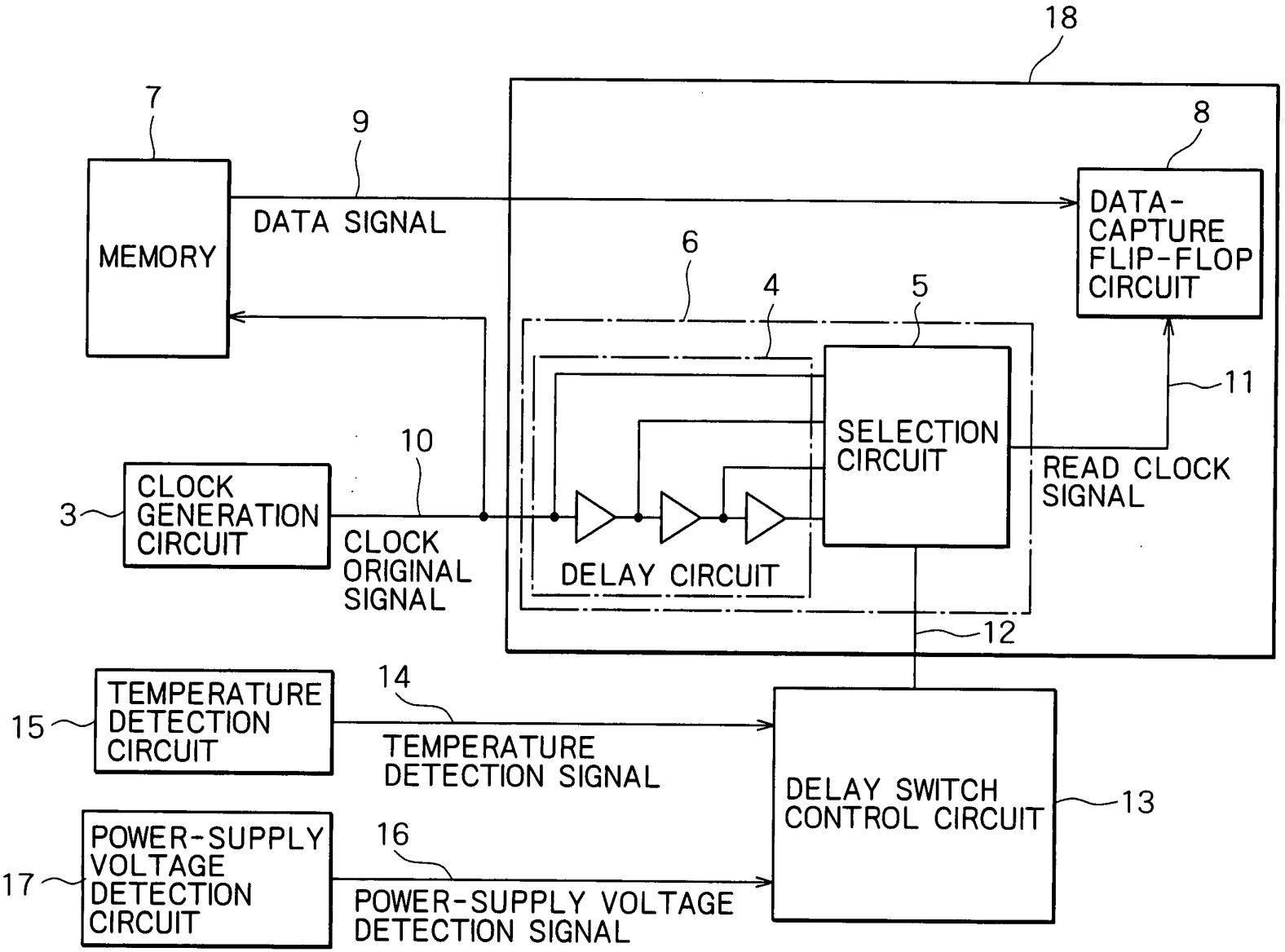

18
7
9
8
MEMORY
DATA SIGNAL
DATA-CAPTURE FLIP-FLOP CIRCUIT
6
4
5
11
SELECTION CIRCUIT
READ CLOCK SIGNAL
10
3
CLOCK GENERATION CIRCUIT
CLOCK ORIGINAL SIGNAL
DELAY CIRCUIT
12
15
TEMPERATURE DETECTION CIRCUIT
14
TEMPERATURE DETECTION SIGNAL
DELAY SWITCH CONTROL CIRCUIT
13
17
POWER-SUPPLY VOLTAGE DETECTION CIRCUIT
16
POWER-SUPPLY VOLTAGE DETECTION SIGNAL

FIG. 13

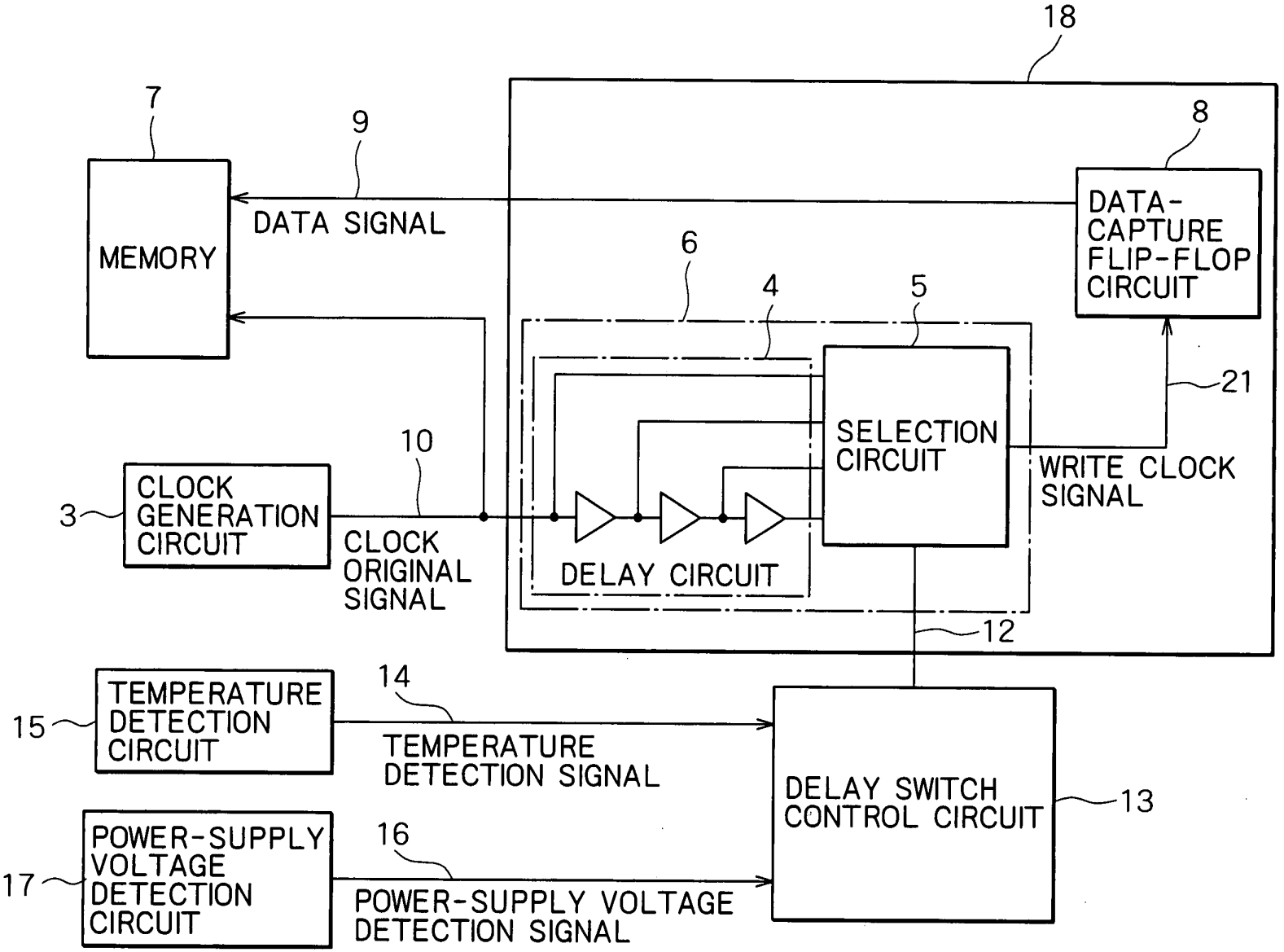

18
7
9
8
MEMORY
DATA SIGNAL
DATA-CAPTURE FLIP-FLOP CIRCUIT
6
4
5
21
SELECTION CIRCUIT
10
3
CLOCK GENERATION CIRCUIT
CLOCK ORIGINAL SIGNAL
WRITE CLOCK SIGNAL
DELAY CIRCUIT
12
14
15
TEMPERATURE DETECTION CIRCUIT
TEMPERATURE DETECTION SIGNAL
DELAY SWITCH CONTROL CIRCUIT
13
16
17
POWER-SUPPLY VOLTAGE DETECTION CIRCUIT
POWER-SUPPLY VOLTAGE DETECTION SIGNAL

FIG. 14

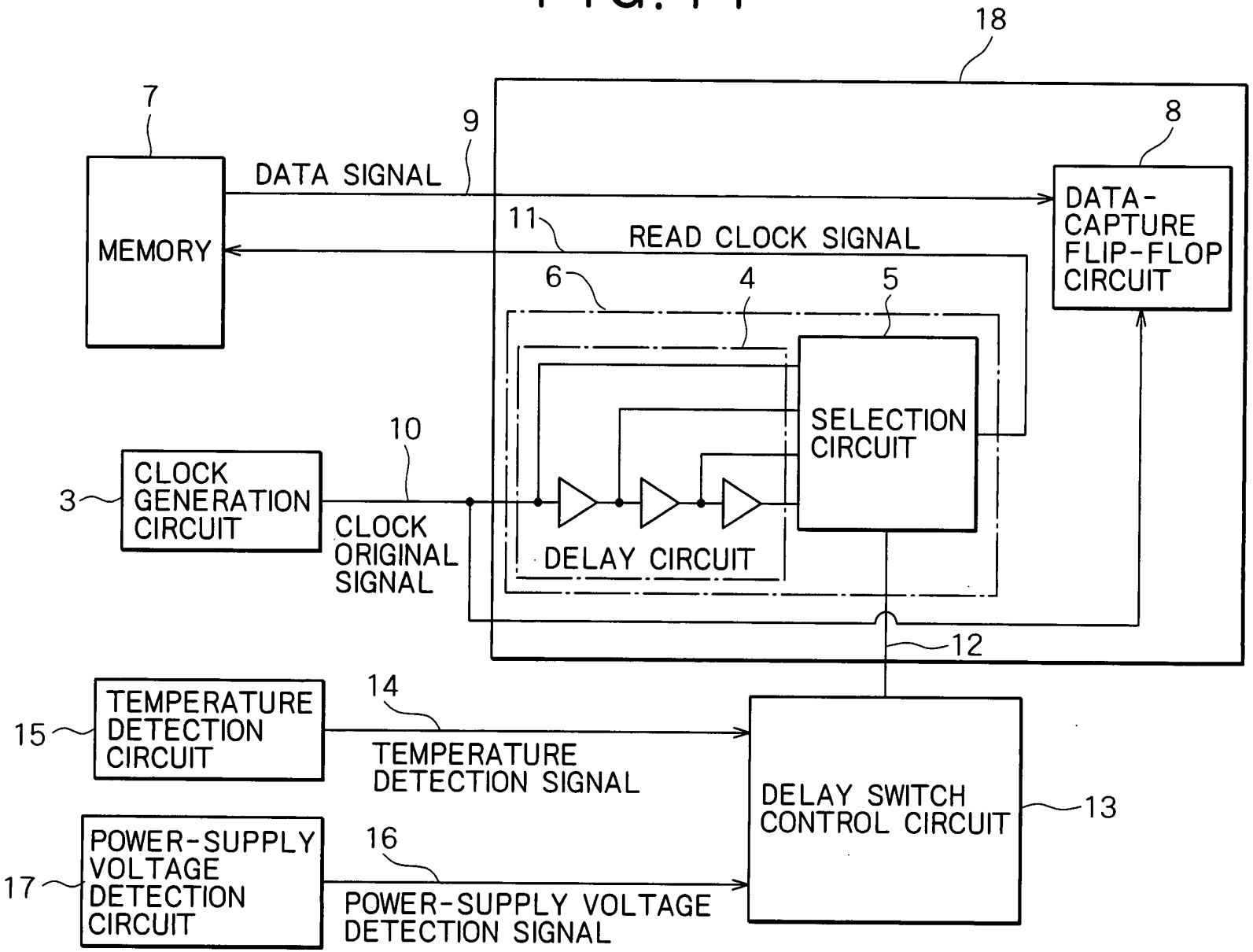

18
7
9
8
DATA SIGNAL
MEMORY
DATA-CAPTURE FLIP-FLOP CIRCUIT
11
READ CLOCK SIGNAL
6
4
5
SELECTION CIRCUIT
10
3
CLOCK GENERATION CIRCUIT
CLOCK ORIGINAL SIGNAL
DELAY CIRCUIT
12
14
15
TEMPERATURE DETECTION CIRCUIT
TEMPERATURE DETECTION SIGNAL
DELAY SWITCH CONTROL CIRCUIT
13
16
17
POWER-SUPPLY VOLTAGE DETECTION CIRCUIT
POWER-SUPPLY VOLTAGE DETECTION SIGNAL

FIG. 15

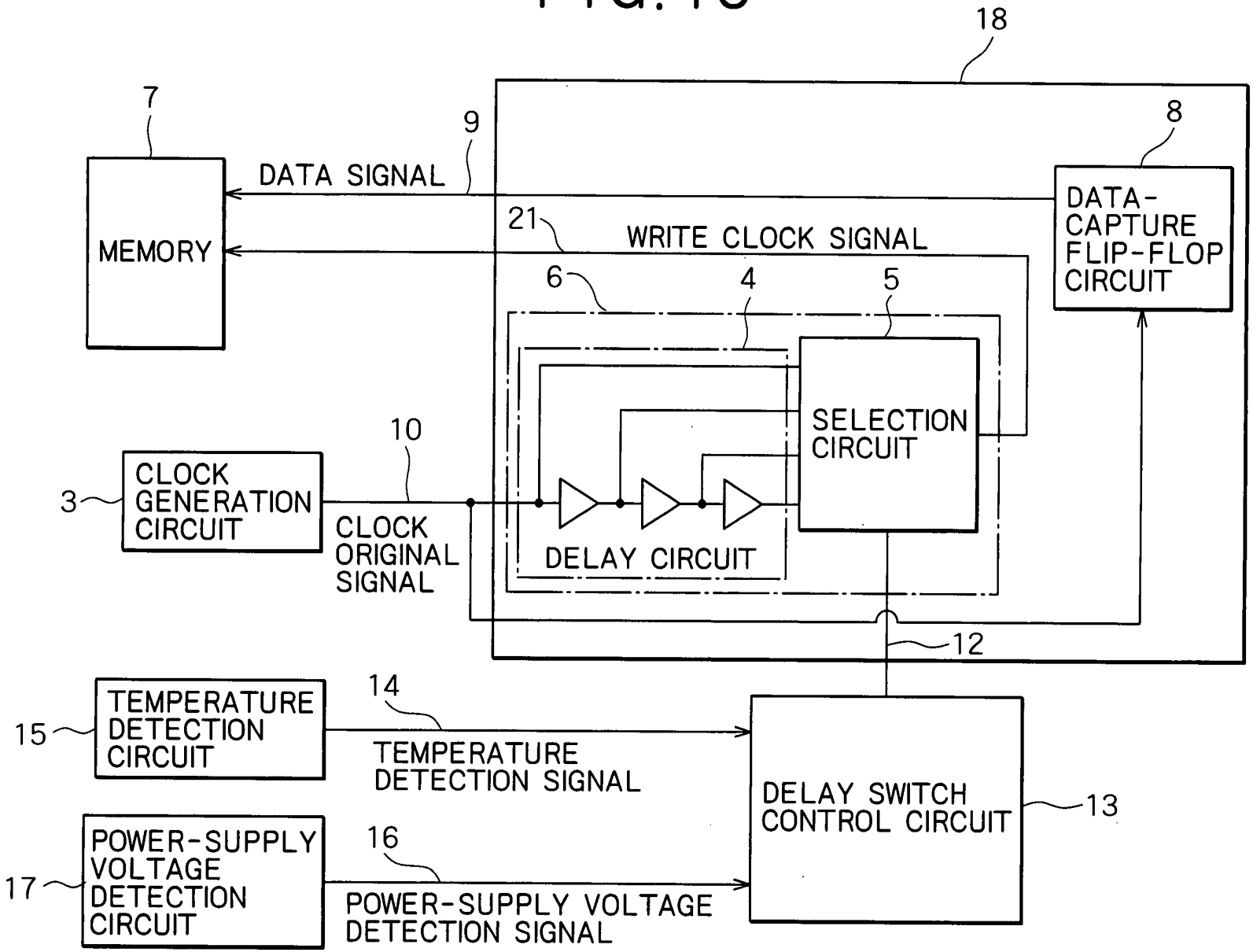

18
7
9
8
DATA SIGNAL
MEMORY
DATA-CAPTURE FLIP-FLOP CIRCUIT
21
WRITE CLOCK SIGNAL
6
4
5
SELECTION CIRCUIT
10
3
CLOCK GENERATION CIRCUIT
CLOCK ORIGINAL SIGNAL
DELAY CIRCUIT
12
14
15
TEMPERATURE DETECTION CIRCUIT
TEMPERATURE DETECTION SIGNAL
DELAY SWITCH CONTROL CIRCUIT
13
16
17
POWER-SUPPLY VOLTAGE DETECTION CIRCUIT
POWER-SUPPLY VOLTAGE DETECTION SIGNAL

FIG. 16

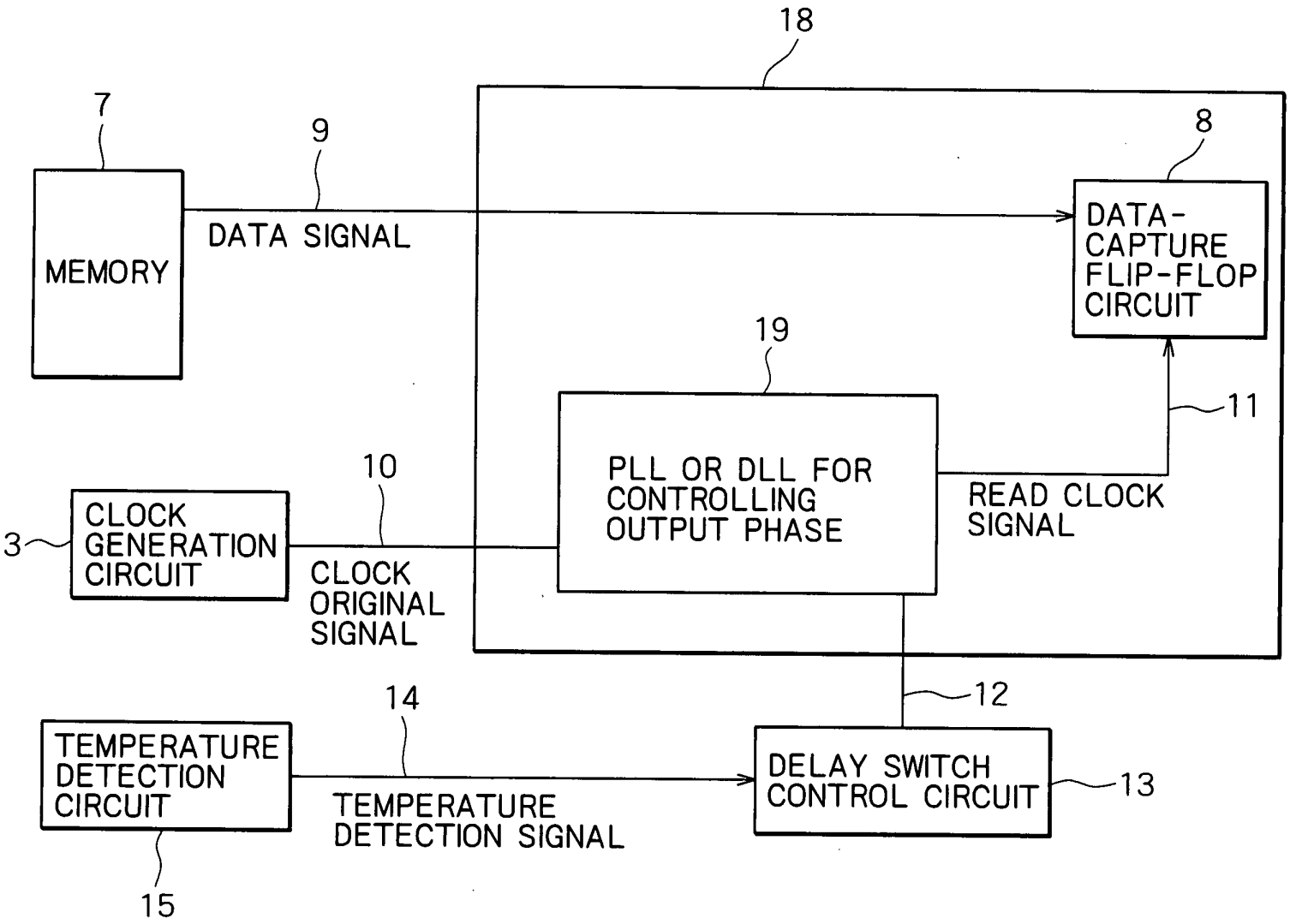

18
7
9
8
MEMORY
DATA SIGNAL
DATA-CAPTURE FLIP-FLOP CIRCUIT
19
11
10
PLL OR DLL FOR CONTROLLING OUTPUT PHASE
READ CLOCK SIGNAL
3
CLOCK GENERATION CIRCUIT
CLOCK ORIGINAL SIGNAL
12
14
TEMPERATURE DETECTION CIRCUIT
DELAY SWITCH CONTROL CIRCUIT
13
TEMPERATURE DETECTION SIGNAL
15

FIG. 17

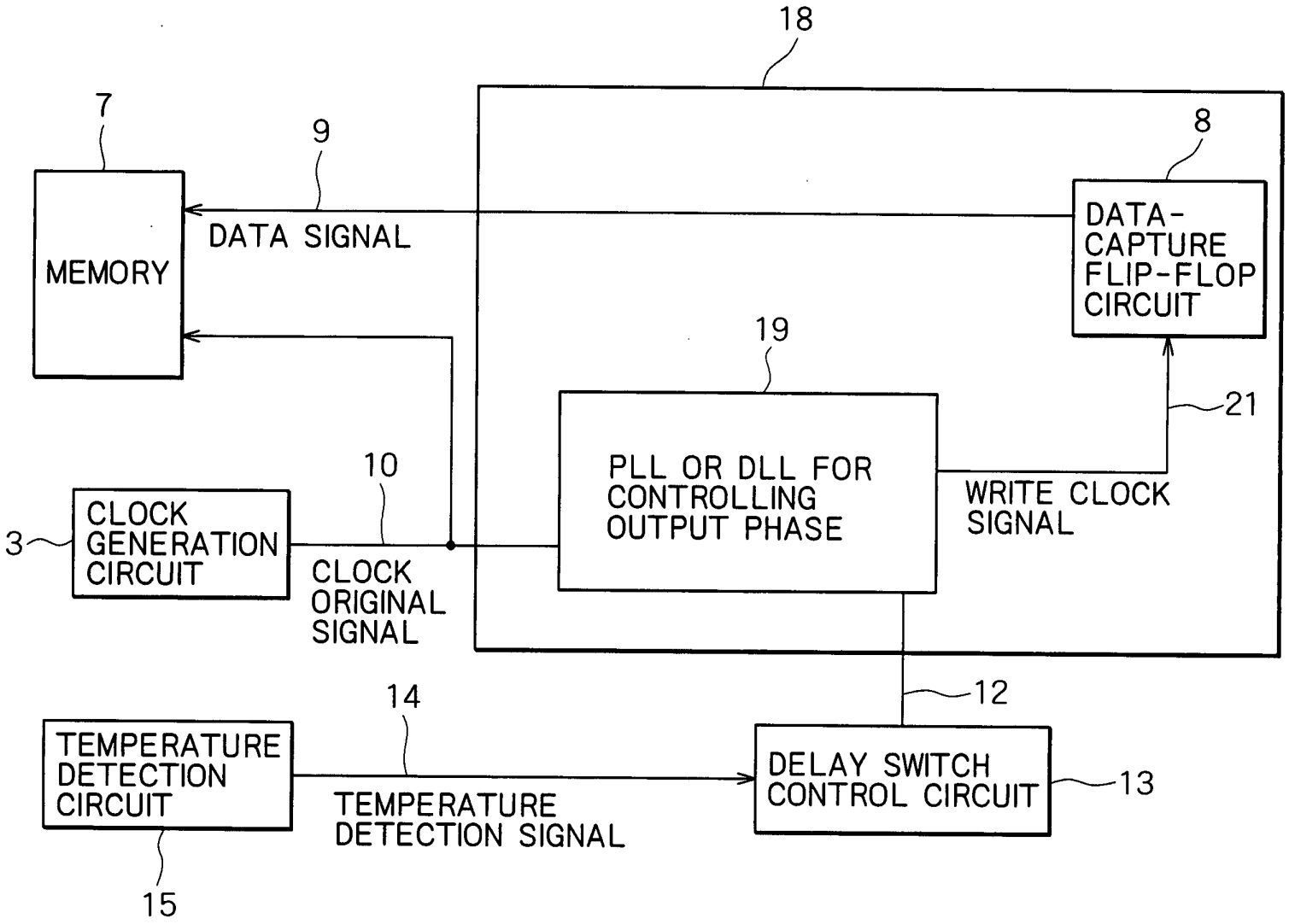

18
7
9
8
MEMORY
DATA SIGNAL
DATA-CAPTURE FLIP-FLOP CIRCUIT
19
21
10
PLL OR DLL FOR CONTROLLING OUTPUT PHASE
WRITE CLOCK SIGNAL
3
CLOCK GENERATION CIRCUIT
CLOCK ORIGINAL SIGNAL
12
14
TEMPERATURE DETECTION CIRCUIT
DELAY SWITCH CONTROL CIRCUIT
13
TEMPERATURE DETECTION SIGNAL
15

FIG. 18

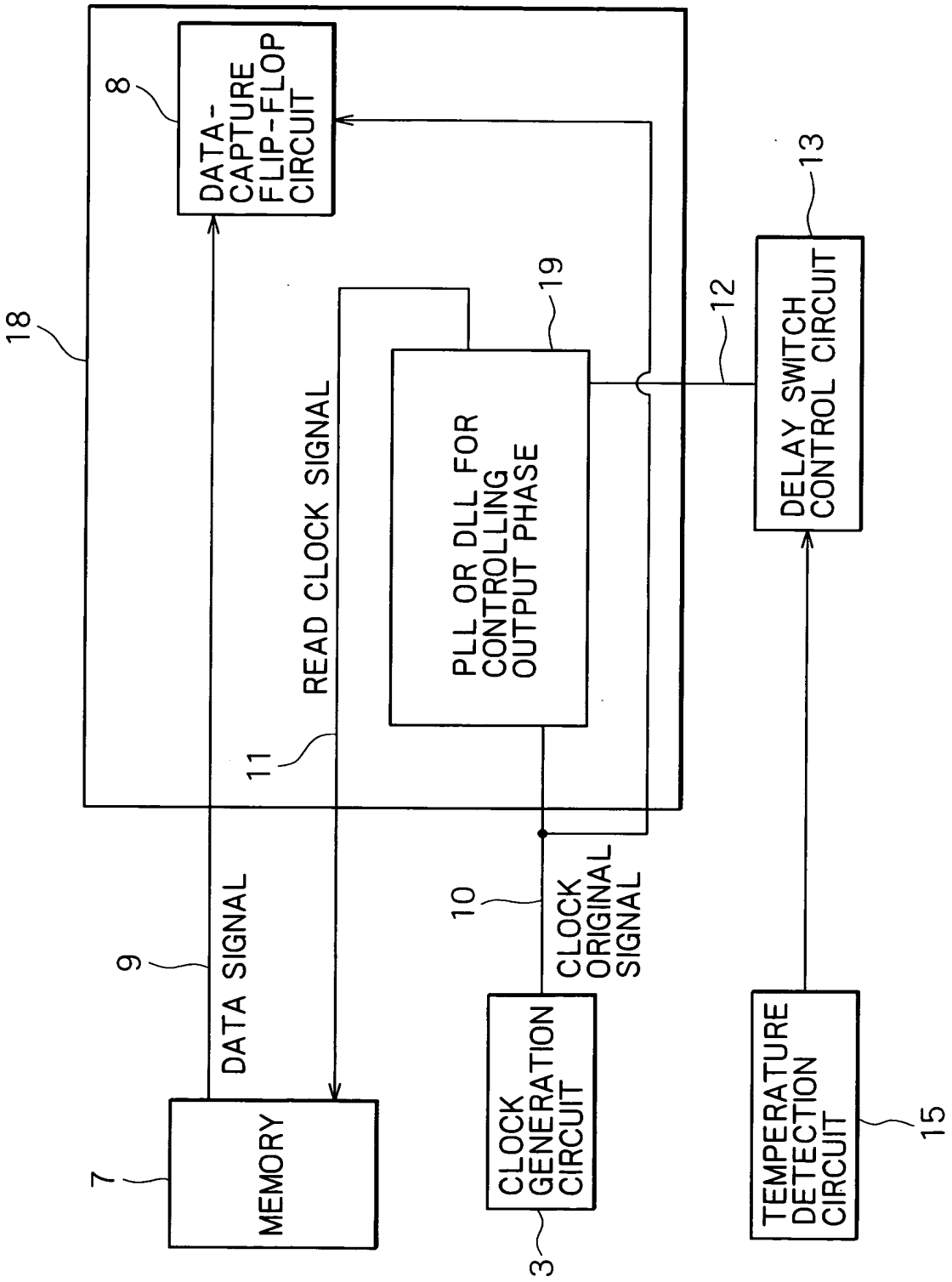
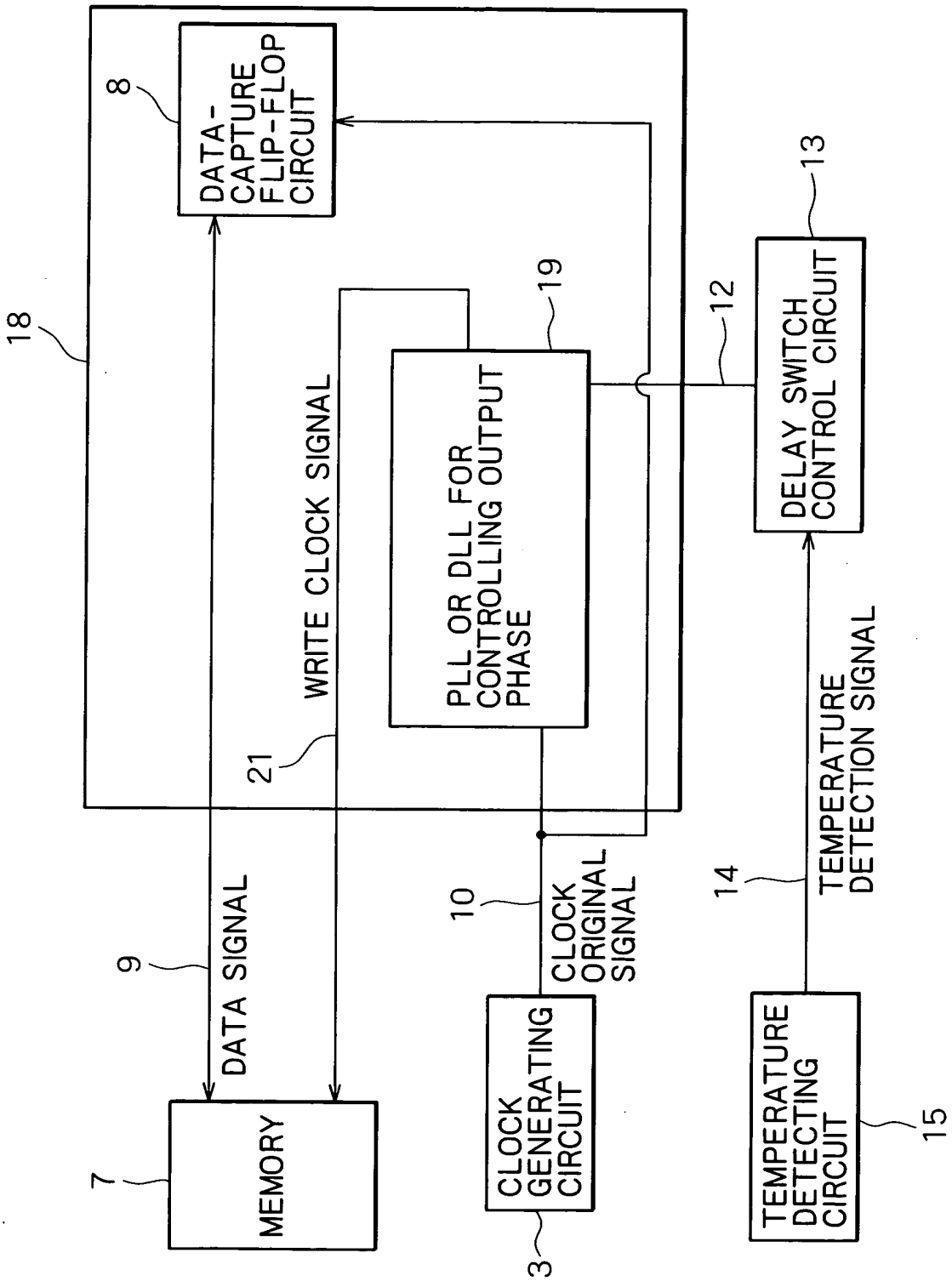

18
8
DATA-CAPTURE FLIP-FLOP CIRCUIT
19
PLL OR DLL FOR CONTROLLING OUTPUT PHASE
12
13
DELAY SWITCH CONTROL CIRCUIT
READ CLOCK SIGNAL
11
9
DATA SIGNAL
10
CLOCK ORIGINAL SIGNAL
7
MEMORY
CLOCK GENERATION CIRCUIT
3
TEMPERATURE DETECTION CIRCUIT
15

FIG. 19


18
8
DATA-CAPTURE FLIP-FLOP CIRCUIT
19
PLL OR DLL FOR CONTROLLING OUTPUT PHASE
12
13
DELAY SWITCH CONTROL CIRCUIT
21
WRITE CLOCK SIGNAL
9
DATA SIGNAL
10
CLOCK ORIGINAL SIGNAL
14
TEMPERATURE DETECTION SIGNAL
7
MEMORY
CLOCK GENERATING CIRCUIT
3
TEMPERATURE DETECTING CIRCUIT
15